REMARKS

Claims 1-17 are pending with claims 13-17 withdrawn from consideration. By this Amendment, claims 1, 6 and 9 are amended for cosmetic purposes only. No new matter is added. Applicants do no disclaim any equivalent of any amended limitation. Applicants appreciate the indication of patentable subject matter in claims 5-7. However, Applicants assert that all of the claims are directed to patentable subject matter for the reasons set forth below.

The Office Action rejects claim 1-4 and 8-12 under 35 U.S.C. §102(e) over Taguchi et al. (U.S. Patent No. 6,438,055). This rejection is respectfully traversed.

In particular, Applicants assert that Taguchi does not teach or suggest a semiconductor memory device that includes a memory array having a plurality of memory cells, a refresh timer circuit providing a refresh request, a command generation circuit generating an internal command signal according to an access command and a row selection control circuit having a timing control circuit rendered active according to the internal command signal, a **timing control circuit** rendered active in response to said internal command signal to **output a timing signal** of a row selection operation of said memory cell, and a **refresh timing control circuit** rendered active in response to said internal refresh command signal to output said **timing signal** *instead of the timing control circuit*, as recited in independent claim 1.

Taguchi discloses a dynamic memory circuit with an automatic refresh function. See, Abstract. As depicted in Fig. 3, the memory circuit can include a number of memory banks **BANK0** and **BANK1**, an input buffer **10**, a command decoder **12**, the address buffer **14**, a data input/output buffer register **16**, and the refresh address counter **22**. The memory banks **BANK0** and **BANK1** each include memory block **BLK**, row decoder **RDEC**, memory cell array **MC**, sense amplifier **SA**, column decoder **CDEC**, sense buffer/write amplifier **SB/WA**, selector **28**

and command latch **24**. The memory circuit further includes a refresh timer **21**, which periodically generates refresh signal **REF1**, and a refresh command generation circuit **25** that subsequently receives **REF1**. See, Fig. 3 and col. 7, lines 26-44.

In the normal operation mode (as well as the power down mode), the refresh command generation circuit **25** checks the status of the read and write signals **RD** and **WR** provided by command latch **24** and generates an internal refresh command **REF** if (1) no internal operation is already under execution and (2) refresh timer **21** has generated an active refresh time signal **REF1**. In response to this internal refresh command **REF1**, the control circuit **26** will execute a refresh operation for the address memory block **BLK** specified by the refresh address counter **22**. See, col. 7, lines 45-56.

Taguchi does not teach or suggest a **timing control circuit** rendered active in response to an internal command signal to output **a timing signal** ..., and a **refresh timing control circuit** rendered active in response to an internal refresh command signal to output the **timing signal** ***instead*** of the timing control circuit, as recited in independent claim 1. That is, Taguchi does not teach or suggest two separate control circuits that supply a row selection timing signal to a memory cell based on either an internal command signal and refresh command signal.

To the contrary, while the Office Action asserts (on page 3) that Taguchi discloses (1) "a **timing control circuit** (fig. 3, CLK1 received by [command latch] 24) rendered active according to said internal command signal (fig. 3, CMD1) to output timing signals (col. 7, line 60 - col. 8, line 5) of a row selection operation of said memory array" {bolded emphasis added}, and (2) a **refresh control circuit** (fig. 3, [refresh command generation circuit] 25) receiving and holding said refresh request signal (fig. 3, REF) to output said timing signal instead of said timing control circuit" {bolded emphasis added}, Applicants respectfully point out that a review of col. 7, line

60 to col. 8, line 5 (cited by the Office Action) demonstrates that there are no two circuits that generate any single "output timing signal" based on either an internal command signal or a refresh request signal.

A review of Taguchi shows that Taguchi discloses no two circuits that alternately produce any one signal whatsoever. Furthermore, while the Office Action apparently cites Taguchi's control circuit **26** as "rendered active according to said refresh request signal (REF1) to output said **timing signal** ***instead*** of said timing control circuit" {emphasis added}, Applicants point out that the Office Action has identified no particular "timing signal" produced by control circuit **26**, but merely asserts that col. 7, line 60 to col. 8, line 5 of Taguchi discloses such a signal.

In fact, the only viable device in the Taguchi memory that produces anything resembling a timing signal (although not analogous to signals **SO** and **RXT** of the present invention) is command generation circuit **25**, which produces count up signal **S1** and refresh signal **REF**. However, neither of these signals **S1** or **REF** has an alternate source, refresh signal **REF** is clearly recited in another limitation in claim 1 as an "internal refresh command signal" and count up signal **S1** is triggered solely by the falling edge of the refresh signals **REF** of the various Taguchi memory embodiments. See, Fig. 4, 8, 11, 17, 20 and 23. Thus, Taguchi does not teach or suggest each and every limitation of independent claim 1.

Accordingly, independent claim 1 defines patentable subject matter. The dependent claims define patentable subject matter by virtue of their dependency as well as for the additional features they recite. Accordingly, withdrawal of the rejection under 35 U.S.C. §102 is respectfully requested.

For the reasons given above, Applicants believe that this application is in condition for allowance and Applicants request that the Examiner give the application favorable consideration and permit it to issue as a patent. However, if the Examiner believes that the application can be put in even better condition for allowance, the Examiner is invited to contact Applicants' representative listed below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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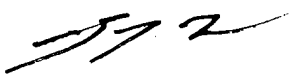

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